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AF/2811-H

TRANSMITTAL OF APPEAL BRIEF (Large Entity)	Docket No. N17-073A

Application Of: **Schroeder et al.**

Serial No.	Filing Date	Examiner	Group Art Unit
09/389,826	**09/03/1999**	**Nadav, O.**	**2811**

Invention: **SEMICONDUCTOR DEVICE**

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **November 12, 2003**

The fee for filing this Appeal Brief is: **$330.00**

☒ A check in the amount of the fee is enclosed.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☒ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **500999**

Signature

Dated: **January 12, 2004**

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I certify that this document and fee is being deposited on **01/12/2004** with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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DOCKET NO. N17-073A

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Schroeder et al.	)	Examiner: Nadav, O.
	)	
Application No.: 09/389,826	)	Art Unit: 2811
	)	
Filed: 09/03/1999	)	
	)	
For: SEMICONDUCTOR DEVICE	)	

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Alexandria, VA 22313-1450

BRIEF OF APPELLANTS

This is an appeal from the Final Rejection dated August 11, 2003, rejecting claims 1-9. This Brief is accompanied by the requisite fee set forth in 37 C.F.R. §1.17 (c).

REAL PARTY IN INTEREST

U.S. Philips Corporation is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

As filed, this case included claims 1-5. Claims 6-9 were added in the Amendment filed September 14, 2001. Claims 1-9 remain pending, stand rejected, and form the basis of this appeal. No claims have been allowed.

STATUS OF AMENDMENTS

An After-Final Amendment has not been filed in response to the Final Action mailed August 11, 2003.

SUMMARY OF THE INVENTION

The present invention provides a semiconductor device having a semiconductor body which on a surface comprises an integrated circuit containing protection means for protection against electrostatic discharge (ESD). The protection means comprises a compound element of an SCR and a gated diode, the protection means being provided in a surface area of a first conductivity type having a well of a second, opposite, conductivity type, wherein a surface zone of the first conductivity type forms a first anode and cathode area of the SCR element, wherein the surface area has a surface zone of the second conductivity type, further denoted as first zone, situated remote from the well and forming a second anode and cathode area of the SCR element, and wherein the gated diode contains a gate insulated from the surface of the semiconductor body and a

highly-doped second conductivity type surface zone aligned to this gate further denoted as second zone, which second zone partly overlaps the well of the second conductivity type. The second zone stretches out only along a part of the periphery of the well, the first zone is provided along at least another part of this periphery of the well which is free from the second zone, and an anode and cathode of the SCR element in the first zone are not shielded from one another by the gated diode. Because the anode and cathode of the SCR element are not shielded from one another by the gated diode, load carriers injected by the cathode can reach the anode more easily, which results in a considerably lower holding voltage than in known devices.

ISSUES

Whether claims 1-6 and 9 are anticipated under 35 U.S.C. § 102(b) by U.S. Patent No. 5,572,394 (Ker et al.).

Whether claims 7-8 are unpatentable under 35 U.S.C. § 103(a) over Ker et al.

GROUPING OF CLAIMS

Claims 1-9 stand or fall together.

ARGUMENT

The rejections based on Ker et al., hereafter "Ker," are defective because Ker fails to teach or suggest each and every feature of the claims as required by 35 U.S.C. §§ 102 and 103.

Ker fails to disclose, *inter alia*, the claimed first and second zones and gated diode having a gate, wherein the second zone is "aligned to this gate," "said second zone stretches out only along a part of the periphery of the well, the first zone is provided along at least another part of this periphery of the well which is free from the said second zone," and "an anode and cathode of the SCR element in the first zone are not shielded from one another by the gated diode." Ker's failure to disclose these features is clearly evidenced by the layout shown in FIG. 11 of Ker, and the cross-sectional view of FIG. 11 illustrated in FIG. 9 of Ker. In particular, from FIG. 11 of Ker, it appears that any potentially analogous regions in the Ker structure are co-extensive along their corresponding n-wells. In sharp contrast, FIGS. 4-6 of the claimed invention clearly show a second zone (e.g., 17) that "stretches out only along a part of the periphery of the well" (e.g., 11), and a first zone (e.g., 14, 19) that "is provided along at least another part of this periphery of the well which is free from the said second zone." Accordingly, since Ker fails to disclose each and every feature of independent claim 1 as required by 35 U.S.C. § 102(b), Appellants respectively submit that claim 1 and its dependent claims are allowable.

In light of the above, Appellants submit that claims 1-9 are allowable and respectfully request reversal of the final rejection.

Respectfully submitted,

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APPENDIX

Claim Listing:

1. A semiconductor device having a semiconductor body which on a surface comprises an integrated circuit containing protection means for protection against electrostatic discharge (ESD), the means being a compound element of an SCR and a gated diode, the protection means being provided in a surface area of a first conductivity type having a well of a second, opposite, conductivity type,

wherein a surface zone of the first conductivity type forms a first anode and cathode area of the SCR element,

the surface area has a surface zone of the second conductivity type, further denoted as first zone, situated remote from the well and forming a second anode and cathode area of the SCR element, and

the gated diode contains a gate insulated from the surface of the semiconductor body and a highly-doped second conductivity type surface zone aligned to this gate further denoted as second zone, which the second zone partly overlaps the well of the second conductivity type, characterized in that the said second zone stretches out only along a part of the periphery of the well, the first zone is provided along at least another part of this periphery of the well which is free from the said second zone, and an anode and cathode of the SCR element in the first zone are not shielded from one another by the gated diode.

2. A semiconductor device as claimed in claim 1, characterized in that the gate of the gated diode substantially stretches out only along that part of the periphery of the well along which also the said second zone of the second conductivity type stretches out.

3. A semiconductor device as claimed in claim 2, characterized in that the gated diode is arranged in the form of a MOS transistor which has a further surface zone of the second conductivity type, deposited in the surface area of the first conductivity type, the said second zone forming one of the source/drain zones of the transistor and the said further surface zone forming the other one of the source/drain zones of the transistor, the said first zone of the second conductivity type being situated at a shorter lateral distance from the surface zone of the first conductivity type provided in the well than the said further surface zone.

4. A semiconductor device as claimed in claim 3, characterized in that the further zone of the second conductivity type and the said first zone of the second conductivity type form a zone of the second conductivity type.

5. A semiconductor device as claimed in claim 1 characterized in that the first and the second conductivity type are the p-conductivity type and n-conductivity type respectively, the said first zone forming the cathode of the SCR element and the

first conductivity type zone arranged in the well forming the anode of the SCR element.

6. The semiconductor device of Claim 1, wherein the well of the second conductivity type is arranged in the form of a longitudinal zone, the surface zone of the first conductivity type is formed by a longitudinal zone in the well of second conductivity type which well has in its center an opening at the position of which a highly doped zone of the second conductivity type is provided which forms a contact area for the well of second conductivity type.

7. The semiconductor device of Claim 6, wherein the gated diode is provided on one end of the longitudinal zone and comprises the insulated gate and the highly doped second conductivity type surface zone which partly overlaps the well of the second conductivity type.

8. The semiconductor device of Claim 7, wherein the gated diode is arranged as a MOS transistor having a further zone of the second conductivity type.

9. The semiconductor device of Claim 7, wherein the cathode of the SCR is provided along the part of the periphery of the well of the second conductivity type that is free from the gated diode.